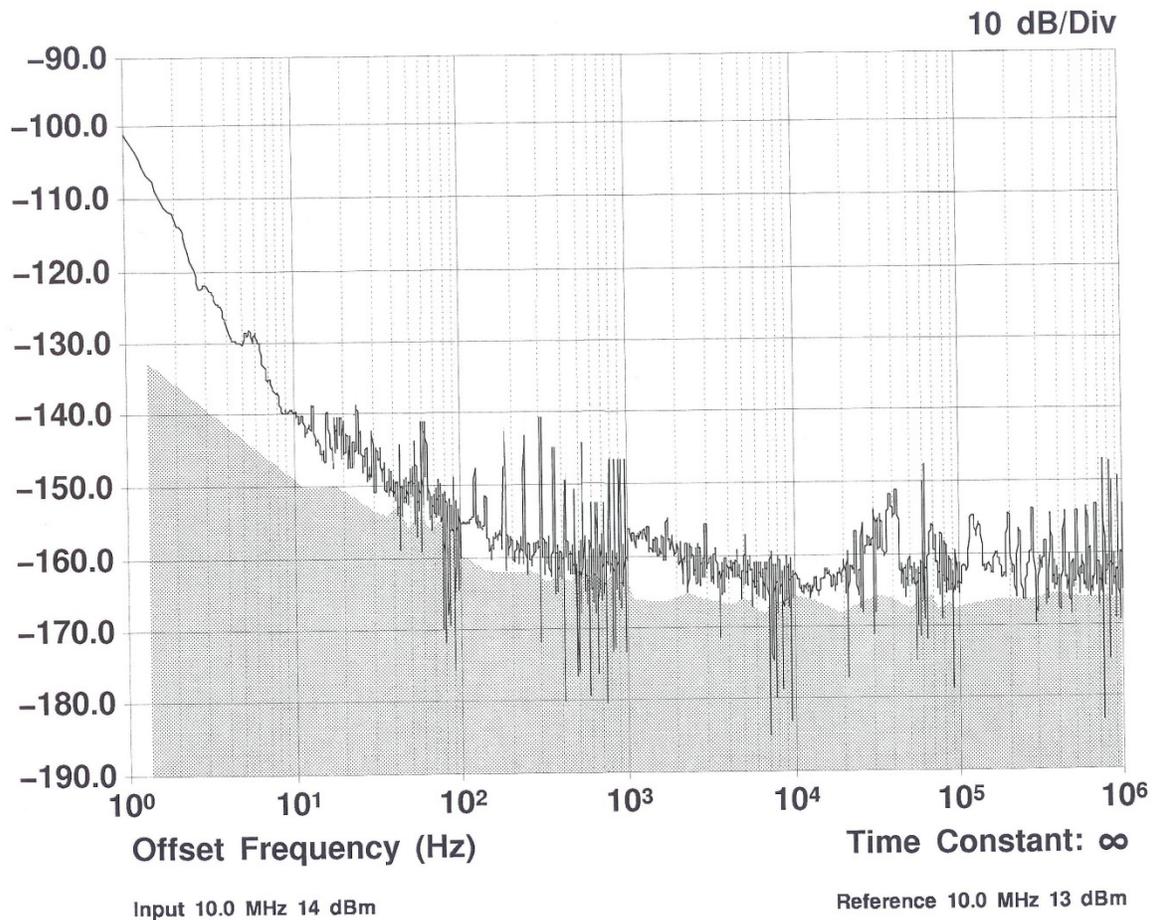


Designing for Exceptional Phase Noise and Jitter Performance in Precision GPS Frequency Standards

17 Dec 2009 22:18:46
1m

$\mathcal{L}(f)$ Phase Noise at 10.0 MHz (dBc/Hz)

TSC 5120A-01



Introduction

This paper addresses the considerations and steps required to design a high performance, low noise precision frequency standard, with particular focus on phase noise and jitter.

Phase Noise and Jitter are different ways of measuring the noisiness of a signal. Both measures are useful in different applications and jitter can be directly calculated from phase noise if the phase noise characteristic is known.

As the two measures are directly linked, we will focus on Phase Noise for the purposes of this paper.

1. Generation of a Low Phase Noise Source

1.1. Selecting a Suitable Crystal Oscillator

Ultimately, the phase noise performance achievable from the instrument is limited by the performance of the internal oscillator deployed to generate the RF frequency (typically 10MHz). An in depth analysis of the many and varied types of oscillators available is beyond the scope of this paper, however it is important to understand the key criteria used to select an appropriate component.

In general, although some of the oscillator characteristics can be compensated in the overall design, the better the oscillator, the better the achievable performance. In this respect invariably the selection will come down to a high performance Oven Controlled Crystal Oscillator (OCXO) or in some instances where the application requires, a double oven version.

The key characteristics of general interest in a frequency standard are;

1.1.1. Good Temperature Stability.

1.1.2. Low aging characteristic.

1.1.3. Low Phase Noise

For this paper we will focus on the last item, low phase noise. Phase noise is typically characterized by the noise at a particular frequency offset, relative to the carrier frequency, in a 1Hz measurement bandwidth, the unit of measure being dBc/Hz.

A good OCXO will have a phase noise characteristic of at least -125 dBc/Hz at a 10Hz offset from a 10MHz carrier, and at higher offsets will fall more or less linearly to a noise "floor" (the point at which no further improvement can be seen) of less than -160 dBc/Hz at a 10kHz offset from a 10MHz carrier.

Note: In evaluating phase noise specifications, it is critical to know at what carrier frequency the measurement is quoted, as there is a direct mathematical relationship between carrier frequency and measured phase noise as shown below:

$$\text{phase noise at } f_1 = \text{phase noise at } f_2 + 20 \log_{10} n$$

where $n = f_1 / f_0$.

For example, if phase noise is quoted for a 5MHz carrier, the effective phase noise at 10MHz could be determined from;

$$\text{phase noise @ 10MHz} = \text{phase noise @ 5MHz} + 20 \log_{10} 2 = \text{phase noise @ 5MHz} + 6 \text{ dBc}$$

Therefore, if a phase noise of -125 dBc is quoted for a 10Hz offset from a **5MHz** carrier, the phase noise for a 10Hz offset at **10MHz** cannot mathematically be better than -119 dBc !

2. Preservation of Low Phase Noise when Buffering and Distributing.

2.1. Introduction

Once we have a high quality output, the next step is to interface this to the outside world, without compromising the quality of the original signal. This requires careful layout, buffering and filtering as described below.

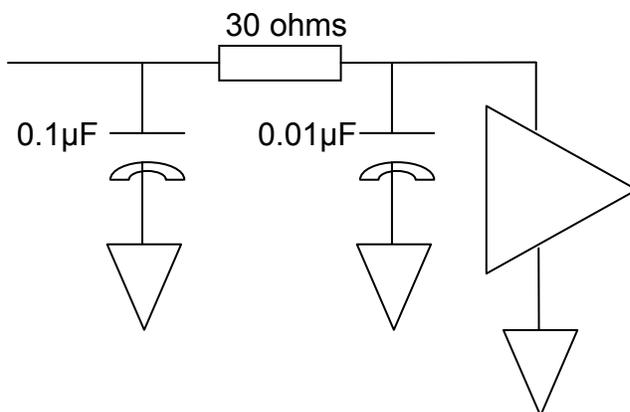
2.2. Power Supplies

Nowadays, one of the most common ways of converting from an AC mains supply input is to use a DC-DC converter. This generally has the advantage that it can cover a wide range ("universal") of input supplies, often ranging from 100VAC to 265VAC. Unfortunately, a side effect of these supplies is that they can be notorious "noise generators" and therefore adequate power supply filtering is a must to preserve phase noise.

Amplitude variations in the supply line can make their way into sensitive circuit paths and produce unwanted sidebands in the phase noise domain. The power supply "noise" is converted from Amplitude Modulated (AM) to Phase Modulated (PM) at points inside the IC's used.

For example, all diode junctions have a built in capacitance which changes depending on the bias voltage. A change in this bias voltage due to power supply "noise" will generate a phase change proportional to the "noise" level and show up on the phase noise data.

In order to achieve a good level of filtering, not only should the supply be filtered at the input to the pcb, but additional filtering placed physically at the supply pins to the buffer amplifiers themselves is advisable, see example below;



2.3. Amplifier Stability

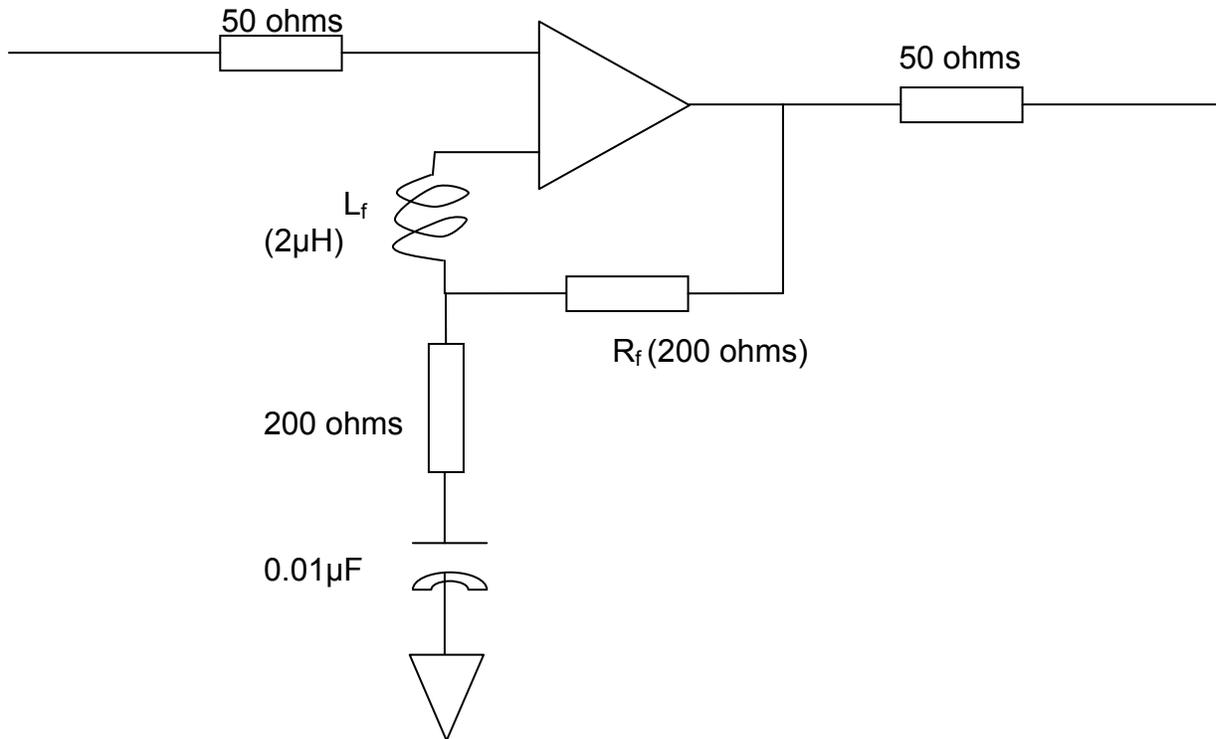
The stability of the amplifiers used in designing buffering and distribution circuits can also have a significant detrimental impact on the phase noise. In addition, unwanted capacitance to ground of a gain stage can cause high frequency peaking of its transfer function. This frequency peaking amplifies the noise within the region of the peak and can result as a peak in the phase noise data usually at the noise floor.

For amplification and distribution of low phase noise RF signals, current feedback amplifiers do a good job, with the understanding that a correct layout is critical to obtaining the desired performance.

These current feedback amplifiers can have bandwidths in the GHz, so bandwidth limiting for the particular application is important. If this aspect of the design is done incorrectly, the impact on the phase noise floor is that it will be much poorer than good be attained with an ideal design.

Also, once again, capacitance to ground at the inputs and outputs can be very detrimental to performance and needs to be reduced as much as possible to avoid instability.

An example of a typical amplifier design is shown below, with the accompanying equation for calculation of desired bandwidth and component values;



For the above example, the bandwidth between 3 dB points is defined by;

$$3\text{dB BW} = \frac{Z_0 F_a}{Z_f} \quad \text{Where:}$$

Z_0 = DC Trans impedance of the amplifier (specified on the amplifier data sheet)

F_a = Dominant open loop pole (specified on the amplifier data sheet)

Z_f = Effective impedance of R_f and L_f

i.e. $Z_f = R_f + 2\pi f L$

In the above equation, if R_f is small, then Z_f will be dominated by L_f . Typical values are shown in parenthesis for a 60MHz 3dB bandwidth, when:

$Z_0 = 110\text{dB}\Omega$ (316k Ω) and $F_a = 200\text{kHz}$.

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